EE 117B/217B Microwave and Wireless Measurements

Lab 7 - Radar

Fall 2026

CAUTION: READ THIS PAGE CAREFULLY BEFORE STARTING THE LAB

This class uses the FieldFox Microwave Analyzer N9918B as the primary instrument. In this lab it will be operated mainly in its Spectrum Analyzer (SA) mode. Along with the FieldFox, this lab uses the Analog Devices EV-ADF4159EB1Z PLL evaluation board (operated as an FMCW chirp generator), DC power supplies, an oscilloscope, and several other RF components. Please handle the instruments very carefully as they are **very expensive** and delicate. The most vulnerable parts of the instruments are the RF PORTS (APC-3.5 connectors). These connectors are protected by the small Female-Female Port Savers, which are the silver ferrules attached to the ports. **DO NOT REMOVE THE PORT SAVERS FROM THE FIELDFOX PORTS FOR ANY EXPERIMENT.**

All connections are to be made through these Port Saver Connectors. If you have never handled RF instrumentation before, ask the instructor to demonstrate how to make connections and handle these connectors and cables. Always hold the cable with one hand (non-dominant) and rotate the end nuts of the SMA cables with the other (dominant) hand. Once you make a soft connection by hand, use the torque wrench provided to complete the connection. Note that whenever SMA connections are made, you must only rotate the end nuts and not the components; this ensures the internal pin enters and exits the jack in a straight trajectory. As far as pushing the control knobs and keys on the instrument are concerned, no special care is needed (they are fail-safe). The worst that can happen is that the instrument may lock up. In that case, press the `Preset` key or ask the instructor for help.

Caution for this particular lab

The PLL evaluation board is powered from two external DC supplies: 5.5 V (board and VCO, red/black banana jacks) and 15 V (loop-filter op-amp, `+15V` and `AGND1` test loops). Check the voltage, polarity and current limit of every supply *before* connecting it to the board. Never apply more than 5.5 V to the banana jacks and never apply any DC supply to the `VTUNE`, `EXT_VCOOUT` or `VCO/2` SMA connectors. The board is ESD sensitive: handle it by its edges and do not touch the VCO, the ADF4159 or the loop-filter components while the board is powered. **In Experiment 2 the op-amp supply is lowered to 12 V and shared with the RF amplifier (ZX60-123LN-S+).** Set and verify the voltage and current limit with the output off, and double-check the polarity before connecting the amplifier.

Introduction

Frequency-modulated continuous-wave (FMCW) radar is the dominant architecture for short-range mmWave sensing: automotive radar, industrial distance sensors, gesture and vital-sign sensing, and imaging radars all use it. An FMCW radar transmits a *chirp*, a signal whose instantaneous frequency is swept linearly over a bandwidth B in a time T_{ramp}. The echo from a target at range R returns delayed by $\tau = 2R/c$; mixing the echo with the transmitted chirp produces a *beat* tone at $f_b = \beta\tau$, where $\beta = B/T_{\text{ramp}}$ is the chirp slope. The range resolution of the radar is set by the swept bandwidth, $\Delta R = c/(2B)$, and the linearity and phase noise of the chirp directly set how clean the beat spectrum (and hence the range profile) is. The chirp generator is therefore the main component of an FMCW radar.

In Lab 4 you characterized the Analog Devices **EV-ADF4159EB1Z** board as a VCO and a phase-locked loop. The ADF4159 is in fact a dedicated *FMCW chirp generator*: in addition to locking the VCO at a fixed frequency, its fractional-N divider can be stepped automatically by an on-chip ramp engine, so that the locked loop sweeps the VCO through a precisely controlled, highly linear chirp. In this lab you will use the board as the chirp source of a radar. In Experiment 1 you will connect and configure the PLL board, program a sawtooth chirp, and measure the chirp on the FieldFox spectrum analyzer. In Experiment 2 you will build a complete FMCW radar around the chirp generator and test it with a coaxial delay line, and in Experiment 3 you will operate the radar over the air with antennas and real targets. The chirp parameters and their relation to the ADF4159 registers are summarized in Appendix A, and the interpretation of a chirp on a swept spectrum analyzer in Appendix B.

Objectives

At the end of this lab you will:

1. Program the ADF4159 PLL as an FMCW chirp generator and compute the ramp register values (`CLK1`, `CLK2`, `DEV`, `DEV offset`, number of steps) for a specified chirp bandwidth and duration.
2. Characterize the chirp in the time domain (`VTUNE`, flyback and cycle slipping) and in the frequency domain on a swept spectrum analyzer, and understand how the RBW and trace settings affect the displayed chirp spectrum.
3. Build a homodyne FMCW radar from a power divider, an amplifier, a mixer and a low-pass filter, and verify its power budget (LO drive level).
4. Measure the beat frequency produced by a known delay and relate it to the delay and the chirp slope.
5. Operate the radar over the air, detect a target, and identify sources of leakage in the IF spectrum.
6. Observe target motion much smaller than the range resolution of the radar.

Since students are performing the lab together, please ensure that you **take turns performing the experiments.**

Equipment List

Table 1 lists the instruments, sources, components, and devices under test used throughout this lab. Verify that all items are present at your bench and in your Lab Box before beginning, and consult the instructor if anything is missing or damaged. Start by reading the user guide of the evaluation board (UG-383) and the datasheets of the ADF4159 and the HMC515 VCO listed in Appendix D; you will need their specifications and maximum ratings throughout the lab.

Lab Report

Each lab comes with a Lab Questionnaire. As you go through this Lab Manual, you will encounter several questions along the way. When you do, go over to that question in the Lab Questionnaire and answer it accordingly. The list of questions and answers will be turned in as your Lab Report. All students in one lab group will submit one combined lab report. **It is recommended that you complete the post-processing parts of the lab also during the designated lab hours so you can work together with your team.**

Equipment	**Part Number**	**Qty**
Keysight FieldFox Microwave Analyzer (SA / VNA modes)	N9918B	1
VCO / PLL evaluation board (ADF4159 + HMC515LP5E VCO)	EV-ADF4159EB1Z	1
DC power supply (+6 V and ±25 V outputs)	Agilent E3631A	1
Oscilloscope	Keysight DSOX2014A	1
PC workstation with ADF4158-9 evaluation software and USB cable	NA	1
4-way power divider	ZC4PD-153-S+	1
RF amplifier	ZX60-123LN-S+	1
Frequency mixer	ZX05-24MH-S+	1
Low-pass filter	SLP-1200+	1
10 dB attenuator	NA	1
30 ft coaxial delay line (from Lab 2)	NA	1
Antennas	Fairview	2
Corner reflector	NA	1
SMA coaxial cables	NA	3–4
SMA-to-BNC cables	NA	2
50 Ω matched load / SMA termination	NA	2
Male-Male / Female-Female SMA adapters	NA	3 / 2
Banana-to-banana and banana-to-test-hook cables	NA	2 sets
Multimeter	NA	1
Torque wrench	(shared)	1
USB flash drive	Sandisk	1

Table 1: Equipment used in the Lab 7 Radar experiments.

1 Experiment 1: Generating an FMCW Chirp with the PLL

In this experiment the EV-ADF4159EB1Z is operated as a closed-loop chirp generator. Recall from Lab 4 the architecture of the board: a 100 MHz TCXO provides the reference, the ADF4159 is programmed with an R-divider of 1 so that the phase-frequency detector (PFD) runs at $f_{\mathrm{PFD}} = 100$ MHz, an active loop filter built around an OP-184 op-amp drives the `VTUNE` line, and the HMC515LP5E VCO (11.5–12.5 GHz) closes the loop. The VCO output is available at `EXT_VCOOUT`, while the VCO output *divided by two* is fed back to the ADF4159 (and is also available at the `VCO/2` SMA, which must be terminated in 50 Ω). The default loop filter on the board is designed for $K_{\mathrm{VCO}} = 150$ MHz/V, $f_{\mathrm{PFD}} = 100$ MHz and a charge-pump current of 2.5 mA, giving a loop bandwidth of about 282 kHz and a phase margin of about 48°.

Important: because the ADF4159 sees VCO/2, every frequency you enter in the software (start frequency and ramp deviation) is *half* of the frequency at `EXT_VCOOUT`. A 400 MHz chirp at the VCO output requires a 200 MHz ramp to be programmed into the PLL.

1.1 Connecting and Powering the PLL Board

Perform all connections with the power supplies **OFF**.

1. **Inspect the board.** Place the board on the bench and identify the red/black banana jacks (5.5 V supply), the `+15V` and `AGND1` test loops (op-amp supply), the `EXT_VCOOUT`, `VCO/2` and `VTUNE` SMA connectors, the USB connector, and the red and green LEDs. Compare with the silkscreen (Figure 2) and the evaluation setup (Figures 4 and 5) shown in the UG-383 user guide (Appendix D).

2. **Terminate the `VCO/2` port** with a 50 Ω SMA load. This port must remain terminated for the whole lab.

3. **Set up the 5.5 V supply.** With the supply output disabled and disconnected from the board, set the voltage to 5.5 V and the current limit to 0.5 A. With Output off, connect the supply `+` to the red banana jack and `COM` to the black banana jack.

4. **Set up the 15 V supply.** With the output disabled and disconnected, set the voltage to 15 V and the current limit to 20 mA. Using the banana-to-test-hook cables, connect `+` to the `+15V` test loop and `COM` to the `AGND1` test loop. **Double-check that the hooks cannot touch each other or any neighboring component.** So far, the DC supplies should still remain off.

5. **Connect the RF output.** Connect `EXT_VCOOUT` to FieldFox Port 2 with an SMA cable. Set up the Fieldfox in SA Mode.

6. **Connect the tuning-voltage monitor.** Connect the `VTUNE` SMA to channel 1 of the oscilloscope with the SMA-to-BNC cable. Turn on the Oscilloscope and restore it to `Default Setup`.

7. **Connect the USB cable** from the board to the PC. This turns on the green LED.

8. **Power up.** Turn on the DC supplies. Check the current draw: approximately 150 mA on the 5.5 V supply and approximately 1 mA on the 15 V supply. If either current is far from these values, or the supply is in current limit, turn both supplies off immediately and call the instructor. Verify that the red and green LEDs on the board are on. If the Fieldfox ADC is out of range, auto-scale it.

1.2 Programming the PLL and Verifying Lock

Before generating a chirp, lock the PLL at a single frequency to confirm that the board, loop filter and software are working.

1. Launch the **ADF4158-9 evaluation software** on the PC (it should already be installed, but if it is not, see UG-476 for installation and Appendix D for the download link).

2. In the device selection window, click `ADF4159/ADF4169`, select `USB board (green)` and click `Connect`. Confirm that the status bar at the bottom left of the window reads "Analog Devices RFG.L Eval Board connected" in green. If it is not connected, try disconnecting and reconnecting the USB port on the PC, or try a different port.

3. Open the `Main Controls` tab and verify the following settings (these are the board defaults):

Setting	**Value**
`Reference Frequency`	100 MHz
R-counter / reference doubler / reference divide-by-2	1 / off / off
`PFD Frequency` (calculated)	100 MHz
`Charge Pump Setting`	2.5 mA
`Phase Detector Polarity`	Negative

   The phase detector polarity must be *negative* because the loop filter on the board is an inverting active filter.

4. In the `RF Settings` area, set the `VCO Output Frequency` to **6000 MHz**. Confirm that the `RFout*2 (MHz)` field reads 12000 MHz.

5. Click `Write All Registers`. Registers whose value has changed but has not yet been written are highlighted in green at the bottom of the window; after the write, no register should be highlighted.

6. On the FieldFox, set:

   `Freq/Dist` → `Center` → 12 GHz
   → `Span` → 1 MHz
   `BW` → `Res BW` → 1 kHz

   Place a peak marker on the carrier. Confirm that the line is clean and stable (locked). Record the carrier frequency and power P_c (**Q1.2.1**).

7. Read `VTUNE` on the oscilloscope. Record the DC tuning voltage at 12 GHz and compare it with your V_{tune} vs. frequency curve from Lab 4 (**Q1.2.2**).

8. Now set the `VCO Output Frequency` to **5900 MHz** (11.8 GHz at `EXT_VCOOUT`), write the registers, and confirm lock on the FieldFox (re-center as needed). Record `VTUNE`. This will be the *start frequency* of the chirp.

Reminder: Take turns in doing the experiments.

1.3 Configuring the Chirp

The ADF4159 ramp engine generates a staircase approximation of a linear chirp: every t_{step} seconds the fractional-N word is incremented by a fixed deviation Δf_{step}, for N_{steps} steps, starting from the frequency programmed in the `Main Controls` tab. The loop filter smooths the staircase into a near-linear sweep. The relations between the register values and the chirp parameters are given in Appendix A. Please read Appendix A fully and then proceed with the rest of this section.
You will program the following chirp:

Parameter	**At `EXT_VCOOUT`**	**At the ADF4159 (VCO/2)**
Ramp mode	Continuous sawtooth	
Start frequency f_0	11.8 GHz	5.9 GHz
Bandwidth B	$\approx$ 400 MHz	$\approx$ 200 MHz
Stop frequency	$\approx$ 12.2 GHz	$\approx$ 6.1 GHz
Number of steps N_{steps}	1000	
Step duration t_{step}	1 μs	
Ramp duration T_{ramp}	1 ms	

1. **Pre-compute the register values.** Using Appendix A with $f_{\text{PFD}} = 100$ MHz, compute (a) the product CLK1$\times$CLK2 required for $t_{\text{step}} = 1$ μs (a valid choice is CLK1 = 10, CLK2 = 10), and (b) the deviation word `DEV` and `DEV offset` required for a per-step deviation of 200 kHz at the ADF4159. Assume `DEV offset` is 2. What is `DEV`? Because `DEV` is an integer, the deviation per step cannot be exactly 200 kHz. Report the values you calculated for `DEV` and the resulting actual bandwidth and chirp slope β (**Q1.3.1**). Before proceeding, check with the instructor if the values you calculated are correct since you will need the right values to proceed.

2. Open the `Ramps and Shift-keying` tab. Set `Ramp mode` to `Continuous sawtooth`.

3. Based on the previous calculations, set the `CLK1` divider and, in the `Up Ramp` area, the `CLK2` divider, the number of steps, the deviation word (`DEV`) and the deviation offset (`DEV offset`). The software displays the resulting ramp parameters; check that the calculated deviation per step, step time and total sweep match your hand calculation. If the software rejects your choice of CLK1/CLK2, choose another factorization with the same product.

4. Enable the ramp (`Ramp On`) and click `Write All Registers`. The ramp starts as soon as register R0 is written with the ramp enabled. Every change of a ramp parameter must be written to the device before it takes effect. You can use `Toggle Ramp On/Off` to instantly turn on and off the ramp.

5. **Verify the chirp on the oscilloscope.** Set up the oscilloscope trigger and scaling to see the sawtooth (a simple way is to simply `Auto scale` it). You should see a sawtooth on `VTUNE`: a linear ramp lasting T_{ramp} followed by a fast return to the start voltage. Record the waveform (**Q1.3.2**). What is the ramp period (**Q1.3.3**)?

6. Zoom into the falling edge (flyback) of the sawtooth. The PLL is commanded to jump back 400 MHz in a single step. Describe the transient you observe and estimate how long it takes `VTUNE` to settle at the start frequency. Do you observe Cycle Slipping (you may need to

capture a `Single` waveform)? Save a plot of the cycle slipping (**Q1.3.4**). Why does this flyback interval have to be excluded from the useful part of an FMCW radar chirp (**Q1.3.5**)?

Reminder: Take turns in doing the experiments.

1.4 Measuring the Chirp Spectrum on the FieldFox

A swept spectrum analyzer sweeps its own local oscillator across the span, typically over tens to hundreds of milliseconds, while the chirp repeats every 1 ms. At any instant the analyzer only sees the chirp when the chirp happens to pass through its resolution bandwidth filter. Read Appendix B before proceeding with this section.

1. On the FieldFox (SA mode), set:

   `Freq/Dist` → `Center` → 12 GHz
   → `Span` → 600 MHz
   `BW` → `Res BW` → 1 MHz
   → `Video BW` → Auto

   Leave the trace in `Clear/Write`. Describe the trace you see from one sweep to the next. Why does a single sweep not show a continuous band (**Q1.4.1**)?

2. Set the trace detector to `Peak` and the trace state to `Max Hold`:

   `Trace` → `Trace Detector` → `Positive Peak`
   `Trace` → `State` → `Max Hold`

   Wait until the trace fills in (several sweeps). You should now see a flat-topped spectrum extending from about 11.8 GHz to 12.2 GHz. Save the trace as a CSV file and plot it (**Q1.4.2**). Note that there is a section of spectrum below 11.8 GHz that is not part of the chirp parameters and also lower in power than the flat top. Where does this part of the spectrum come from (**Q1.4.3**)?

3. Compare the level of the flat top with the CW carrier power P_c you recorded in Q1.2.1. Is the chirp power the same as the CW power (**Q1.4.4**)?

4. **Effect of RBW.** Keeping `Peak` detector and `Max Hold`, repeat the measurement with RBW = 3 MHz, 1 MHz, 500 kHz, 100 kHz, 50 kHz and 10 kHz (clear the Max Hold trace after each change by toggling the trace state). For each RBW, record the level of the flat top. Plot the displayed level vs. RBW. Explain why the power level drops when the RBW is lowered. Based on Appendix B, at what RBW do you expect the peak power level to start dropping for the current chirp slope setting (**Q1.4.5**)?

5. **Line structure of a periodic chirp.** Because the chirp repeats every $T_{\text{ramp}} = 1$ ms, its spectrum is not truly continuous but consists of lines spaced $1/T_{\text{ramp}}$. Set the center frequency to 12 GHz, the span to 20 kHz, the RBW to 100 Hz. Return the Trace setting to `Trace Detector Auto` and `State` to `Clr/Wr`. Record the trace and measure the line spacing (**Q1.4.6**).

Reminder: Take turns in doing the experiments.

2 Experiment 2: Building an FMCW Radar System

Now that we have a working chirp generator, we will build an FMCW radar system around it at 12 GHz. The radar uses a homodyne architecture: a power divider splits the chirp into a transmit path and a local-oscillator (LO) path. The LO path is amplified to drive the mixer, while the transmit path passes through a 30 ft coaxial delay line that stands in for the round trip to a target. The mixer multiplies the delayed chirp with the LO chirp to produce a low-frequency beat tone at $f_b = \beta\tau$, which is low-pass filtered and observed on the oscilloscope. Because the delay line is a known and stable "target", it lets us verify the power budget of the receiver and the relationship between delay and beat frequency before going over the air.

2.1 Adding a Power Divider and an Amplifier

Perform all connections with the power supplies **OFF**.

1. Turn off the PLL board DC power supplies and disconnect the SA. Connect the input of the 4-way power divider (ZC4PD-153-S+) directly to `EXT_VCOOUT` using an M-M SMA adapter. Turn on the PLL board and use `Toggle Ramp On/Off` to turn the chirp **OFF**, so that you are looking at a CW signal only. Measure the power coming out of any of the 4 output ports on the SA. Is this enough power to drive the mixer (ZX05-24MH-S+)? Check the datasheet (**Q2.1.1**).

2. Turn off the DC supply to the PLL board. Since the power is too low to drive the mixer (ZX05-24MH-S+), we need to add an amplifier. Since the DC supply of the RF amplifier (ZX60-123LN-S+) is 12 V, we will lower the DC supply of the PLL board op-amp to 12 V and share this supply with the RF amplifier.

   (a) Make sure the DC output is off. Press `Display Limit` and change the output voltage of the 25 V supply to **12 V** with a current limit of **100 mA**. **Double-check these values before connecting the amplifier, otherwise the amplifier will get damaged!**

   (b) Use a second pair of banana-to-test-hook cables and plug them into the back of the existing connections on the DC supply.

   (c) Connect the amplifier to Output 4 of the power divider using another M-M adapter (we want to avoid cable losses). Connect the DC cables to the RF amplifier carefully (**double-check!**).

   (d) Place a 10 dB attenuator at Port 2 of the FieldFox and connect the RF amplifier output to the input of this attenuator using an SMA cable.

   Turn on the DC supplies and measure the power on the SA. Accounting for the loss in the cable (measured directly on the FieldFox in VNA mode) and the 10 dB attenuator, what is the RF power (in dBm) at the output of the amplifier? Is this within the driving range of the mixer (**Q2.1.2**)? Turn off the DC supply.

Reminder: Take turns in doing the experiments.

2.2 Mixer, Delay Line and IF Filter

1. Disconnect the RF cable and connect the mixer LO port directly to the RF amplifier output with an M-M SMA adapter. Use the long delay line (30 ft) to connect Output 1 of the

power divider (which acts as the transmitter) to the RF port of the mixer. This delay line is mimicking free-space propagation. Connect a low-pass filter (SLP-1200+) to the IF port of the mixer. Why do we need this LPF (**Q2.2.1**)? Measure its response separately on the FieldFox in VNA mode to find the rejection at 12 GHz (**Q2.2.2**).

2. Connect the output of the LPF to Channel 2 of the oscilloscope using an SMA-to-BNC cable. Turn on the DC supplies and toggle the chirp **ON**. Trigger the scope using the `VTUNE` signal, similar to Experiment 1. Scale Channel 2 correctly to observe the IF beat signal. Record the waveform (**Q2.2.3**).

2.3 Measuring the Beat Frequency

1. Based on the electrical length of the delay line (measured in Lab 2) and the chirp slope β, what do you expect the IF beat frequency to be (**Q2.3.1**)?

2. To check the frequency of this beat signal, we will perform an FFT. Scale the horizontal axis on the scope so that we are only looking at the rising portion of the chirp (ramp) on both Channel 1 and Channel 2. We do not want to see the downchirp portion. Then take an FFT of Channel 2:

   `Math` $\rightarrow$ `Operator` $\rightarrow$ `FFT`
   `Center` $\rightarrow$ 50 kHz, `Span` $\rightarrow$ 100 kHz

   Place a marker and observe the IF frequency of the beat signal. What is this frequency? Does it agree with your calculation (**Q2.3.2**)?

3. Note that there is a peak close to DC. Where does this peak come from (**Q2.3.3**)?

Reminder: Take turns in doing the experiments.

3 Experiment 3: FMCW Radar Over the Air

In this experiment the delay line is replaced by a pair of antennas, one transmitting and one receiving, and the radar is pointed at real targets. The delay seen by the mixer is now the fixed delay of the antenna cables plus the round-trip propagation time to the target, $\tau = \tau_{\text{cables}} + 2R/c$, so the beat frequency directly encodes the range of the target. You will see that the IF spectrum also contains peaks that do not come from the target, and identifying where they come from is one of the central practical problems of FMCW radar. Finally, you will look at what the radar can sense at scales much smaller than its range resolution.

1. Disconnect the delay line. Does the peak close to DC still exist (**Q3.1**)? This should provide a clue as to where it could be coming from. Connect Output 1 of the splitter to one of the two Fairview antennas using an SMA cable. Connect the RF port of the mixer to the other antenna.

2. On the scope FFT you should now see a second peak close to DC. Where does this peak come from? Carefully place your hand in the small gap between the two antennas. Did the peak get suppressed? Based on this, can you guess where that peak comes from (**Q3.2**)?

3. Place the corner reflector facing the two antennas at a distance of 5 ft. What is the expected beat frequency, and does it match the peak on the oscilloscope (**Q3.3**)? Save and plot the trace and mark the peak corresponding to the corner reflector (**Q3.4**).

4. Slowly move the corner reflector closer to the antennas and notice the phase of the time-domain IF signal change. You cannot see this on the FFT since we are only plotting magnitude.

5. Sit in front of the radar at a distance of around 1 ft. Sit still and breathe deeply. Do you see the time-domain trace changing with your breathing (**Q3.5**)? What is the range resolution of this radar (**Q3.6**)? If the movement due to breathing is much smaller than the range resolution, how are you able to see the fluctuations on the screen (**Q3.7**)?

6. **Optional:** Lastly, we will look at the range-Doppler map. Connect the PC to the Oscilloscope using the provided USB-A to USB-B cable. Check that the instrument is recognized in Keysight Connection Expert. Copy the Resource String from the Connection Expert and replace it in line 5 of the code. Next, expand the horizontal time axis on the scope to 10.0 ms per division, which captures 100 chirps, making one frame. Run the MATLAB code `radar_rd.m`, which computes and plots the range-Doppler map. The processing steps are described in Appendix C. Once live, move the corner reflector or some target in front of the radar and observe the result. Based on the listed parameters, what is the maximum unambiguous velocity and the velocity resolution of this radar (**Q3.8**)?

7. Turn off the instruments, disconnect and return all equipment into the provided box and pack up the FieldFox. This is the last lab in this class, so hope you enjoyed the experiments. Good luck on your course projects.

Reminder: Take turns in doing the experiments.

Appendix

A FMCW Ramp Generation in the ADF4159

The ADF4159 is a fractional-N synthesizer. We did not discuss this in class but essentially it is a PLL whose divider can take on fractional values. It uses a 25-bit number to control the fractional part of the division ratio. With the PLL locked, its output (here, the VCO/2 signal) is

$$f_{\mathrm{PLL}} = f_{\mathrm{PFD}} \left(\mathrm{INT} + \frac{\mathrm{FRAC}}{2^{25}} \right), \qquad f_{\mathrm{VCO}} = 2 f_{\mathrm{PLL}}.$$

The ramp engine adds a programmable increment to the fractional word at a programmable rate. Its parameters are:

Deviation per step. The frequency increment per step, set by the 16-bit deviation word `DEV` and the 4-bit deviation offset `DEV offset`, is

$$\Delta f_{\mathrm{step}} = \frac{f_{\mathrm{PFD}}}{2^{25}} \times \left(\mathrm{DEV} \times 2^{\mathrm{DEV\ offset}} \right). \tag{1}$$

With $f_{\mathrm{PFD}} = 100$ MHz, the deviation resolution with `DEV offset` $= 0$ is $f_{\mathrm{PFD}}/2^{25} \approx 2.98$ Hz.

Step duration. The time between steps is set by the two 12-bit clock dividers `CLK1` and `CLK2`:

$$t_{\mathrm{step}} = \frac{\mathrm{CLK1} \times \mathrm{CLK2}}{f_{\mathrm{PFD}}}. \tag{2}$$

Chirp parameters. With N_{steps} steps per ramp (20-bit register), the ramp duration, swept bandwidth and chirp slope at the VCO output are

$$T_{\mathrm{ramp}} = N_{\mathrm{steps}}\, t_{\mathrm{step}}, \qquad B = 2\, N_{\mathrm{steps}}\, \Delta f_{\mathrm{step}}, \qquad \beta = \frac{B}{T_{\mathrm{ramp}}}, \tag{3}$$

where the factor of 2 accounts for the VCO/2 feedback on the EV-ADF4159EB1Z.

Ramp modes. The ADF4159 supports *continuous sawtooth* (ramp up, jump back to the start frequency, repeat), *continuous triangular* (ramp up, ramp down, repeat), *single sawtooth burst* and *single ramp burst* modes, as well as dual-slope ramps, ramp delay and FSK/PSK superimposed on a ramp. See the ADF4159 datasheet for details.

Loop bandwidth and chirp linearity. The staircase produced by the ramp engine is smoothed by the PLL loop filter. As long as the step duration is short compared with the loop's response time ($t_{\mathrm{step}} \ll 1/f_{\mathrm{BW}}$, with $f_{\mathrm{BW}} \approx 282$ kHz here), the VCO follows a smooth, nearly linear sweep, delayed by a small tracking lag. Abrupt changes (the flyback of a sawtooth, or the turnaround of a triangle) excite the loop's transient response and produce a non-linear interval at the start of each ramp. This large jump in fact induces cycle slipping in the PLL, which we will observe.

B Viewing a Chirp on a Swept Spectrum Analyzer

A swept spectrum analyzer measures the power falling inside its resolution bandwidth (RBW) filter as it slowly sweeps across the span. When the input is a chirp that sweeps much faster than the analyzer, the chirp passes through the RBW filter only briefly, once per chirp period, while the analyzer is tuned to a given frequency. The displayed trace therefore depends on the detector and trace mode:

- With a *sample* or *average* detector and `Clear/Write`, each sweep shows only scattered points where the chirp happened to coincide with the analyzer, or a level well below the chirp power.
- With a *peak* detector and `Max Hold`, the analyzer retains the maximum seen at each frequency bin; after enough sweeps, the trace shows the envelope of the chirp: a flat top spanning the swept bandwidth B.

RBW and the displayed level. A chirp of slope β spends approximately $t_{\text{dwell}} \approx \text{RBW}/\beta$ inside an RBW filter, whereas the filter needs roughly 1/RBW to respond fully. The full chirp power is displayed only when $t_{\text{dwell}} \gtrsim 1/\text{RBW}$, i.e. when

$$\text{RBW} \gtrsim \sqrt{\beta}.$$

For narrower RBW the displayed level drops (approximately in proportion to $\text{RBW}/\sqrt{\beta}$ in amplitude) because the filter never has time to charge up to the full signal amplitude.

Line spectrum. A chirp that repeats exactly with period T_{ramp} is a periodic signal, so its spectrum consists of discrete lines spaced $1/T_{\text{ramp}}$ apart within the swept band. These lines are resolved only when the RBW is well below $1/T_{\text{ramp}}$ and the analyzer dwells long enough on each line.

C FMCW Range-Doppler Processing

The beat signal of one chirp. Consider a target at range R moving with radial velocity v (positive when moving away). For one chirp of slope β, the mixer output after the low-pass filter is approximately a single tone

$$s(t) \approx A\cos(2\pi f_b t + \phi)\,, \qquad f_b = \beta\tau, \qquad \phi = 2\pi f_0 \tau = \frac{4\pi R}{\lambda}, \tag{4}$$

where $\tau = \tau_{\text{cables}} + 2R/c$ is the total delay of the RF path relative to the LO path, f_0 is the start frequency of the chirp and $\lambda = c/f_0$ (≈ 2.5 cm at 12 GHz). The *frequency* of the beat tone encodes range; its *phase* encodes range on the much finer scale of the wavelength.

Fast time and slow time. The radar transmits a train of N_c identical chirps, one every chirp repetition period T_c (here $T_c = T_{\text{ramp}} = 1$ ms and $N_c = 100$, so one frame lasts $N_c T_c = 100$ ms). Time within a chirp is called *fast time*; the chirp index $m = 0, 1, \ldots, N_c - 1$ is called *slow time*. The samples of each chirp are stored as one column of an $N_s \times N_c$ matrix, where N_s is the number of samples per chirp.

Removing the dead zone. Each chirp begins with the flyback of the sawtooth, during which the PLL is still settling (and may cycle-slip) and the beat signal is not a clean tone. The chirp boundaries are found from the falling edges of `VTUNE` (Channel 1), and the first t_{skip} of every chirp is discarded. Only the remaining $T_{\text{ramp}} - t_{\text{skip}}$ of each chirp is processed, so the bandwidth actually used is

$$B_{\text{eff}} = \beta\,(T_{\text{ramp}} - t_{\text{skip}}).$$

Range FFT. A windowed FFT of each column (along fast time) converts the beat frequency into range:

$$R = \frac{c}{2}\left(\frac{f_b}{\beta} - \tau_{\text{cables}}\right), \qquad \Delta R = \frac{c}{2B_{\text{eff}}}, \tag{5}$$

where ΔR is the range resolution. The maximum observable range is set by the sample rate f_s of the oscilloscope: the beat frequency must remain below $f_s/2$. A window (e.g. Hann) is applied before the FFT to lower the sidelobes of strong returns, at the cost of a slightly wider peak.

Doppler FFT. Between consecutive chirps a moving target changes its range by vT_c, so the phase ϕ in Eq. (4) advances by

$$\Delta\phi = \frac{4\pi v T_c}{\lambda}$$

per chirp, while its beat frequency (and therefore its range bin) remains essentially unchanged. In each range bin, the complex values from the range FFT therefore rotate at the Doppler frequency

$$f_D = \frac{\Delta\phi}{2\pi T_c} = \frac{2v}{\lambda}. \tag{6}$$

A second windowed FFT, taken across the N_c chirps (along slow time) in every range bin, separates the returns by velocity. The result, plotted as magnitude versus range and velocity, is the *range-Doppler map*. Stationary objects (walls, the bench, the corner reflector at rest) and the leakage paths you identified in Experiment 3 all have $v = 0$ and appear on the zero-Doppler line.

Velocity resolution and maximum velocity. The Doppler FFT observes the phase rotation for a total time $N_c T_c$ and samples it once per chirp. This gives

$$\Delta v = \frac{\lambda}{2N_c T_c}, \qquad v_{\max} = \pm\frac{\lambda}{4T_c}, \tag{7}$$

where Δv is the velocity resolution and $v_{\max}$ the maximum unambiguous velocity. A target moving faster than $v_{\max}$ rotates by more than π between chirps and aliases to a wrong velocity. Longer frames improve the velocity resolution; shorter chirps increase the maximum velocity.

Zero padding. The MATLAB code zero-pads both FFTs. This interpolates the displayed map on a finer grid and makes peaks easier to locate, but it does not improve the range or velocity resolution, which are fixed by B_{eff} and $N_c T_c$.

D References

Software

- EVAL-ADF4159 Evaluation Board Product Page and Software

- ADF4158-9 PLL Software
- ADIsimPLL PLL Design & Simulation Tool

User Guides

- UG-476: PLL Software Installation Guide
- UG-383: EVAL-ADF4159 Reference Guide

Datasheets

- ADF4159 Frequency Synthesizer Datasheet
- HMC515 VCO Datasheet
- OP184 Operational Amplifier Datasheet