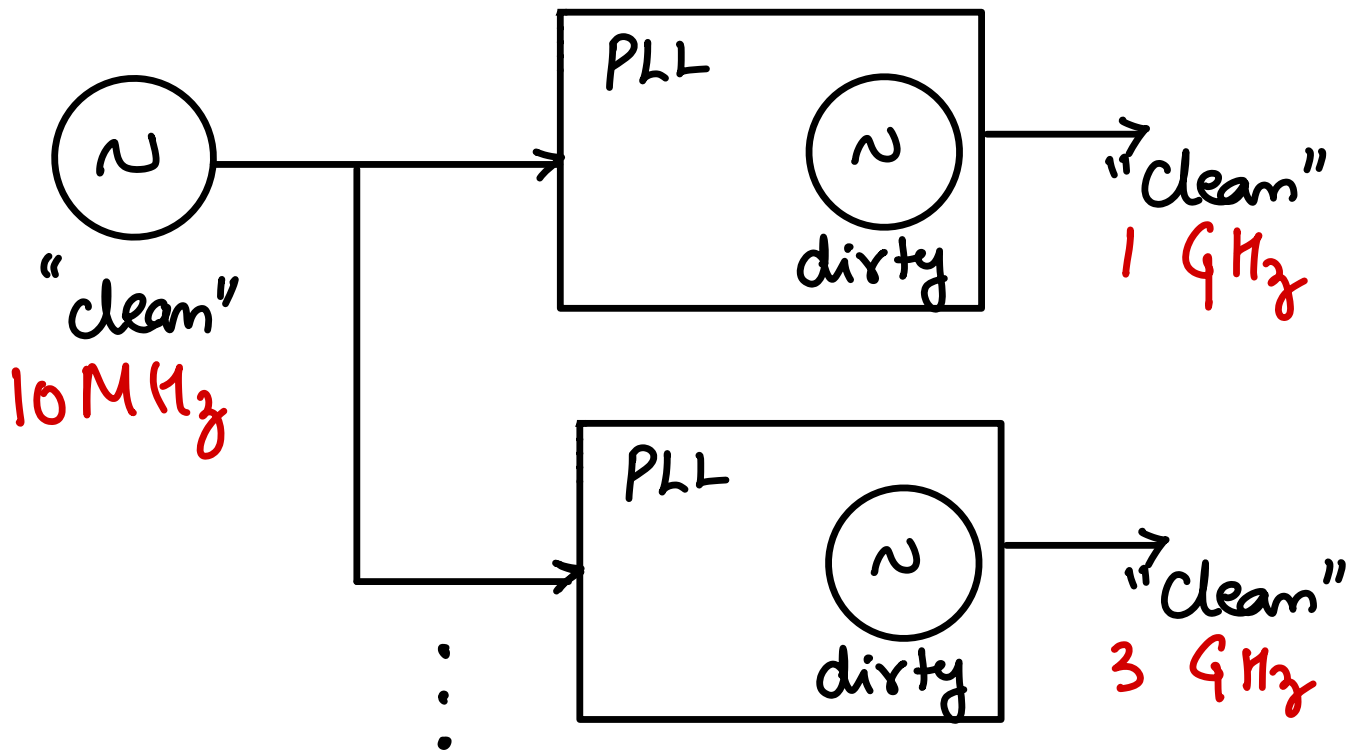




Phase locked loops

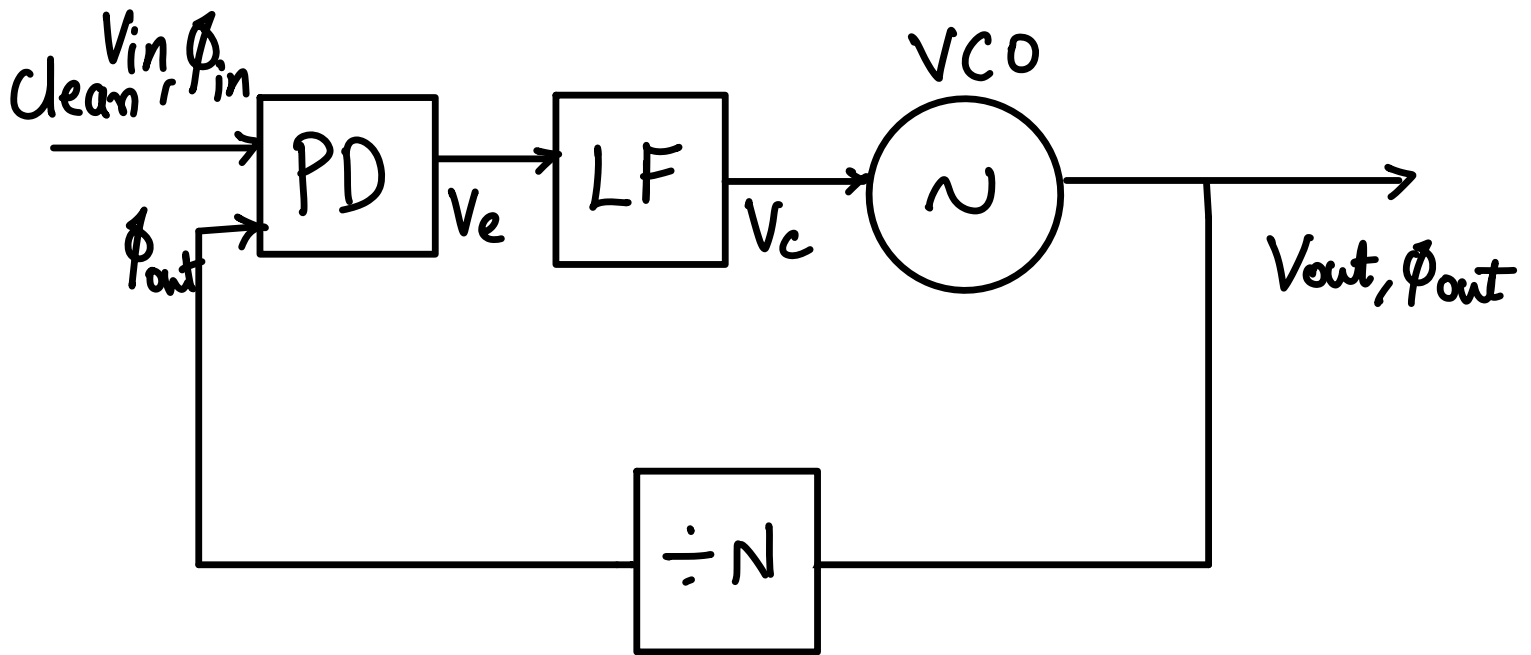
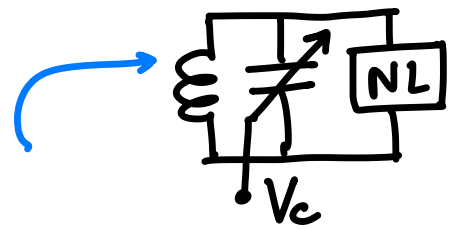
> Given a "clean" source, we can use it to "lock" a "dirty" source.



Advantages

- ▷ Phase coherence
- ▷ Stable frequency
- ▷ PN is better
- ▷ Frequency multiplication.

PLL Architecture



$$V_{in}(t) = A_{in} \sin(\omega_{in} t)$$

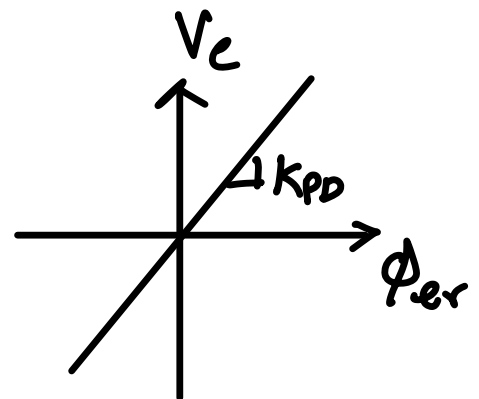
$$V_{out}(t) = A_{out} \sin(\omega_{out} t + \phi_0)$$

$$\Rightarrow \phi_{in} = \omega_{in} t ; \quad \phi_{out} = \omega_{out} t$$

$$\phi_{er}(t) = \phi_{in}(t) - \phi_{out}(t) = (\omega_{in} - \omega_{out})t$$

PD

$$V_e \propto \phi_{er} \Rightarrow V_e = K_{PD} \phi_{er}$$



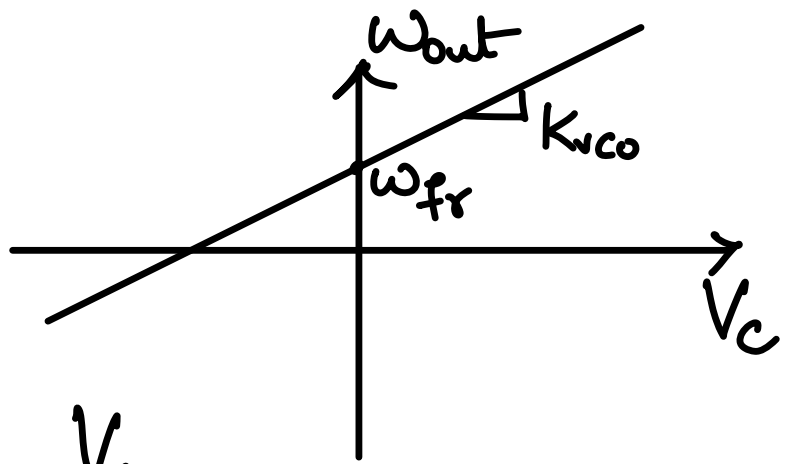
Loop Filter

$$L(s) = \frac{V_c(s)}{V_e(s)}$$

VCO

$$\omega_{out} \propto V_c$$

$$\omega_{out} = \omega_{fr} + K_{vco} V_c$$



$$\phi_{out} = \int \omega_{out} dt$$

$$= \int \omega_{fr} dt + \int K_{vco} V_c dt$$

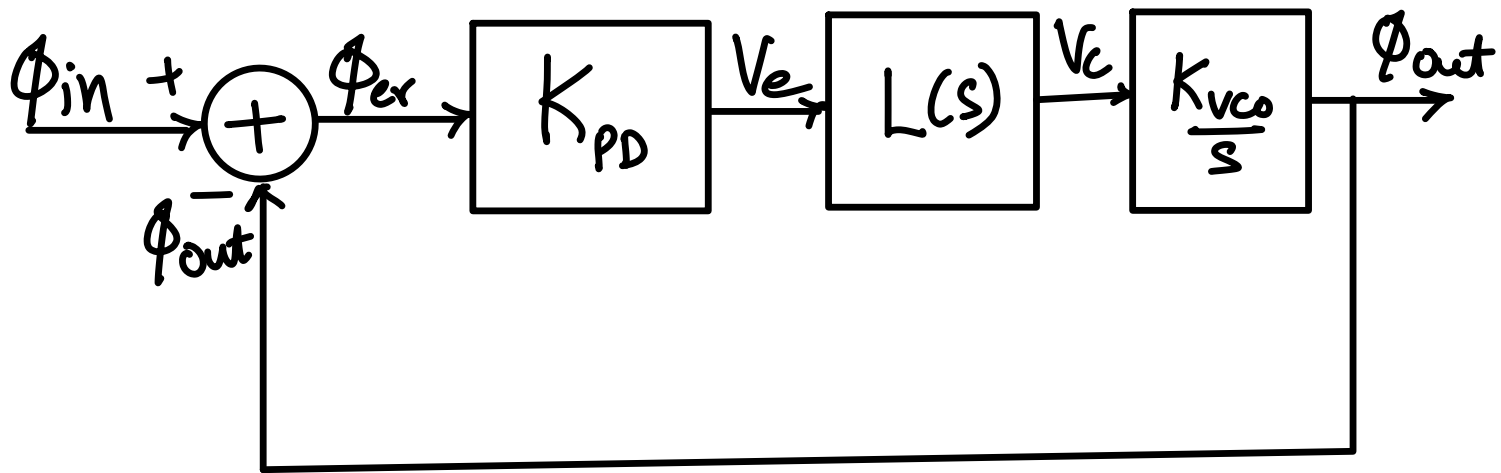
$$\phi_{out} = \omega_{fr} t + K_{vco} \int V_c dt$$

$$\Delta \phi_{out} = K_{vco} \int \Delta V_c dt$$

$$\Rightarrow \frac{\Delta \phi_{out}(s)}{\Delta V_c(s)} = \frac{K_{vco}}{s}$$

Abusing notation, $\frac{\phi_{out}(s)}{V_c(s)} = \frac{K_{vco}}{s}$

Small Signal (linear) Model



$$LG(s) = K_{PD} L(s) \frac{K_{VCO}}{s}$$

$$\phi_{ex}(s) = \phi_{in}(s) - LG(s) \phi_{ex}(s)$$

$$\Rightarrow \boxed{\phi_{ex}(s) = \frac{\phi_{in}(s)}{1 + LG(s)}}$$

$$\text{Locked} \Rightarrow \lim_{t \rightarrow \infty} \phi_{ex}(t) = 0 \text{ (or constant)}$$

$$\text{FVT} \Rightarrow \lim_{s \rightarrow 0} s \phi_{ex}(s) = 0$$

$$\Rightarrow \lim_{s \rightarrow 0} \frac{s}{1 + LG(s)} \cdot \phi_{in}(s) = 0$$

Locking
condition

Type and Order of a PLL

Type: # of integrators in Loop.

Order: # of poles in loop.

Phase Step

$$\phi_{in}(t) = \phi_{in}(0) u(t)$$

$$\Rightarrow \phi_{in}(s) = \frac{\phi_{in}(0)}{s}$$

$$\text{Type 1} \quad LG(s) = \frac{\overbrace{K_{PD} K_{VCO}}^K L(s)}{s}$$

$$\Rightarrow \lim_{s \rightarrow 0} \frac{s}{\frac{KL(s)}{s} + 1} \cdot \frac{1}{s} = 0$$

$\Rightarrow$ Type 1, 2, ... can lock a phase step.

Frequency Step/Phase Ramp

$$\Delta \phi_{in}(t) = \int_{-\infty}^t \Delta \omega_{in}(0) u(t) dt$$
$$= \frac{\Delta \omega_{in}(0)}{s^2}$$

Type ①

$$\lim_{s \rightarrow 0} \frac{\Delta \omega_{in}(0)}{s^2} \cdot \frac{s^2}{s + KL(s)} = \frac{\Delta \omega_{in}(0)}{KL(0)} \neq 0$$

Type ②

$$\lim_{s \rightarrow 0} \frac{\Delta \omega_{in}(0)}{s^2} \cdot \frac{s^3}{s^2 + KL(s)} = 0$$

Frequency Ramp

Type ① X

Type ② $\rightarrow$ const. $\checkmark$

Type ③ $\rightarrow \checkmark$

Type I

- ▷ Phase, Freq step ✓
- ▷ Frequency Ramp ✗

Type II, III

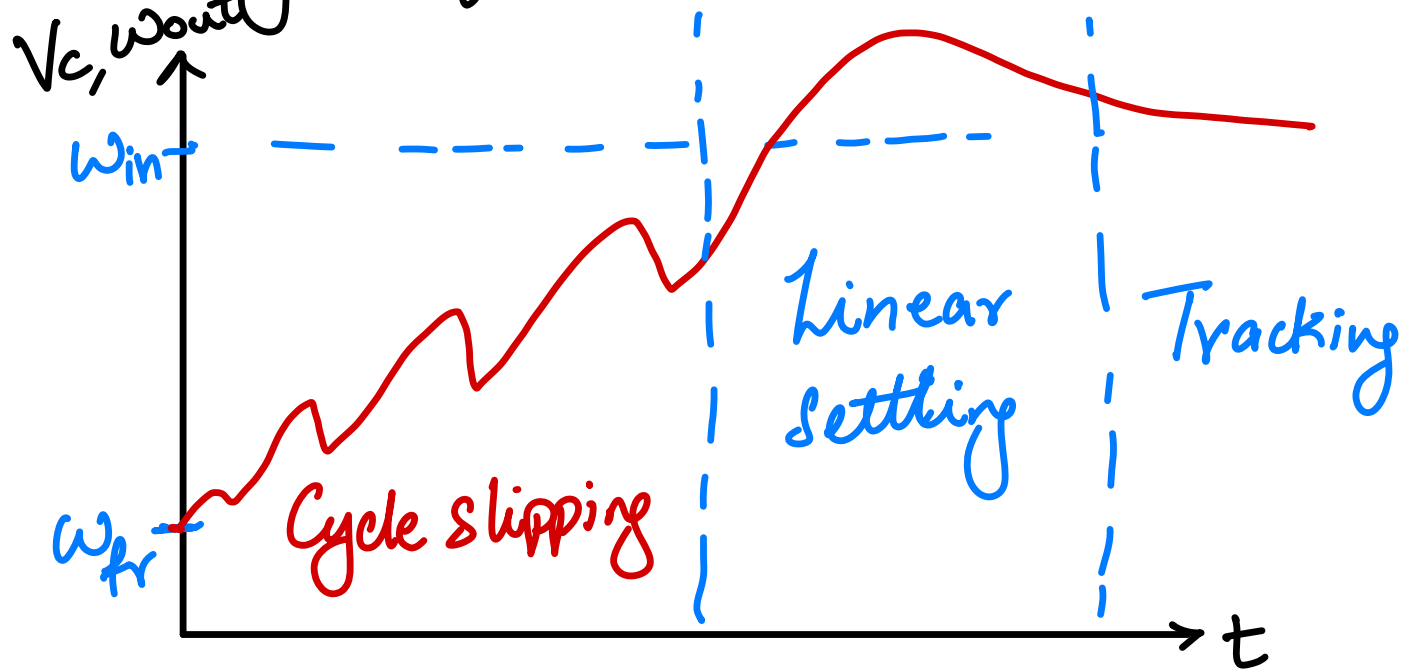
- ▷ Phase, Freq step ✓
- ▷ Fr. ramp ✓

Caution: 2 integrators $\Rightarrow PM = 0^\circ$

Type 2: $LF(s) = \frac{1 + s\tau_p}{s\tau_i}$

Type ① ✗ $\rightarrow$ Cannot lock } Type ②
Type ③ ✗ $\rightarrow$ Unstable } PLLs are a good compromise

Locking Dynamics



Acquisition Ranges

1) Hold-in Range (Δw_H)

▷ Range of frequencies over which PLL maintains lock.

2) Lock-in Range (Δw_L)

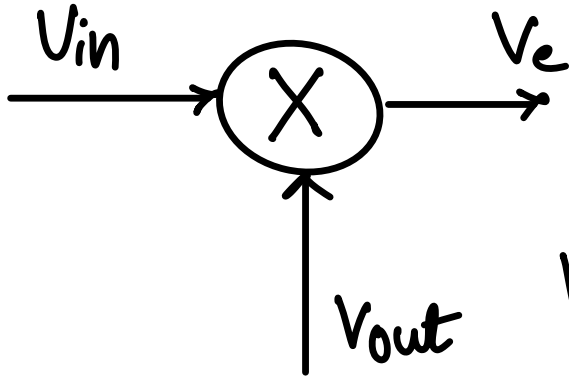
▷ Range of frequencies over which PLL can lock without cycle slipping.

3) Pull-in Range

▷ Range of fr. over which PLL can acquire lock.

$$\Delta\omega_L \leq \Delta\omega_p \leq \Delta\omega_H \leq \Delta\omega_T$$

Phase Detector



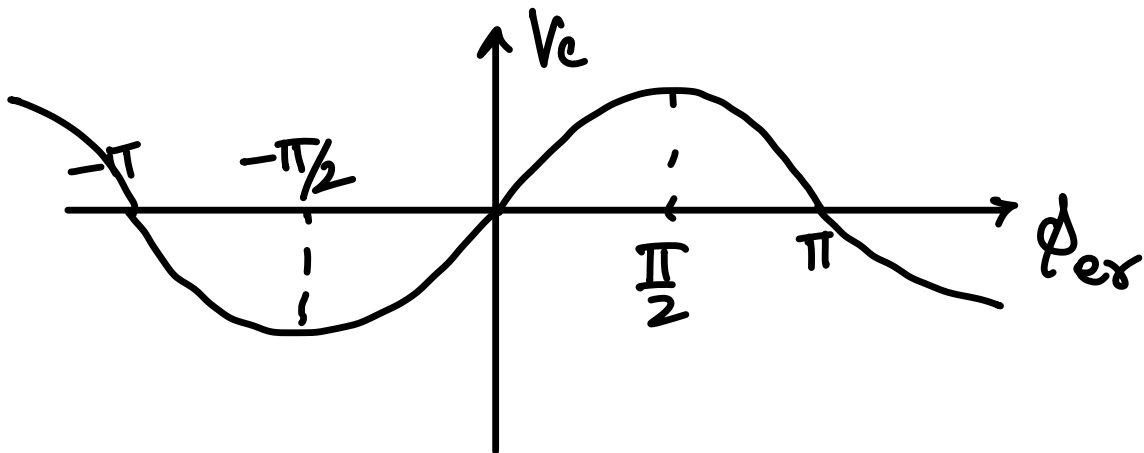
$$V_{in}(t) = A_{in} \sin(\omega_{in}t + \phi_{in}^0)$$

$$V_{out}(t) = A_{out} \cos(\omega_{out}t + \phi_{out}^0)$$

$$V_e(t) = \frac{A_{in} A_{out}}{2} \left[\sin(\omega_{in}t + \omega_{out}t + \phi_{in}^0 + \phi_{out}^0) + \sin[(\omega_{in} - \omega_{out})t + \phi_{in}^0 - \phi_{out}^0] \right]$$

$$\Rightarrow V_e(t) = \frac{A_{in} A_{out}}{2} \sin(\phi_{ex}(t))$$

$$\Rightarrow V_e(t) = \overbrace{\frac{A_{in} A_{out}}{2}}^{K_{PD}} \sin(\phi_{ex}(t))$$



$$K'_{PD} = \frac{dV_e}{d\phi_{ex}} = K_{PD} \cos(\phi_{ex})$$

Non-linear Analysis

$$\frac{d\phi_{er}}{dt} = \frac{d}{dt} (\phi_{in} - \phi_{out})$$

$$= \omega_{in} - \omega_{out}$$

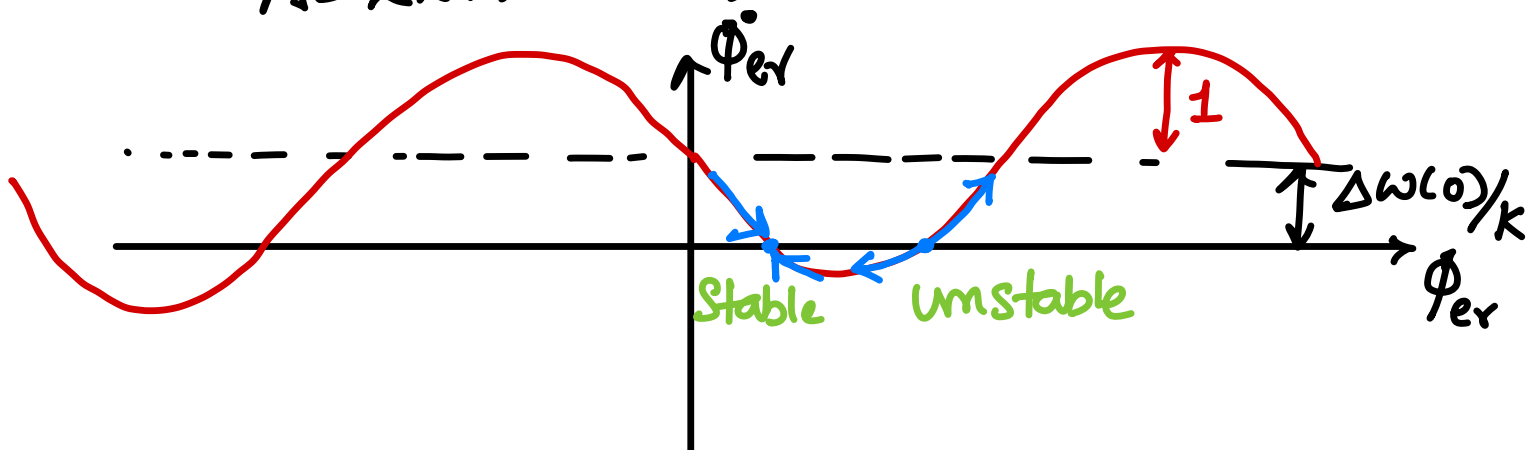
$$= \omega_{in} - (\omega_{fr} + K_{vco} V_c)$$

$$= \Delta\omega(0) - K_{vco} V_c$$

$$\Rightarrow \dot{\phi}_{er} = \Delta\omega(0) - K_{vco} (K_{pd} \sin(\phi_{er}))$$

$$\Rightarrow \boxed{\frac{\dot{\phi}_{er}}{K} = \frac{\Delta\omega(0)}{K} - \sin(\phi_{er})}$$

ADLER'S EQ. OF A PLL



Solution exists when $\Delta\omega(0) < k$

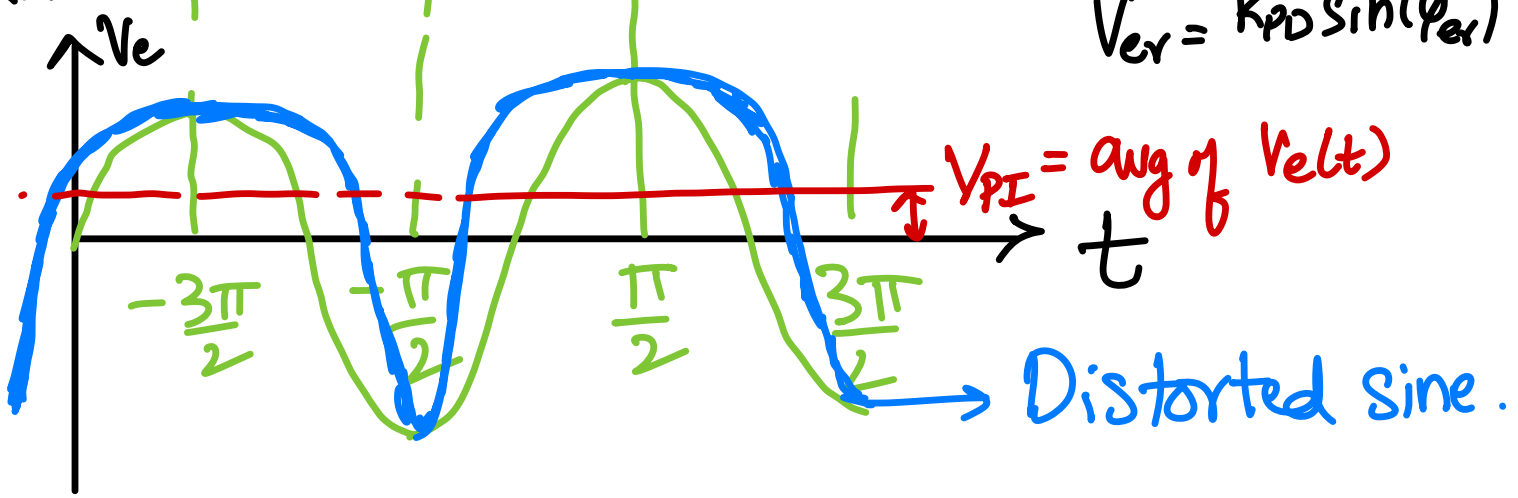
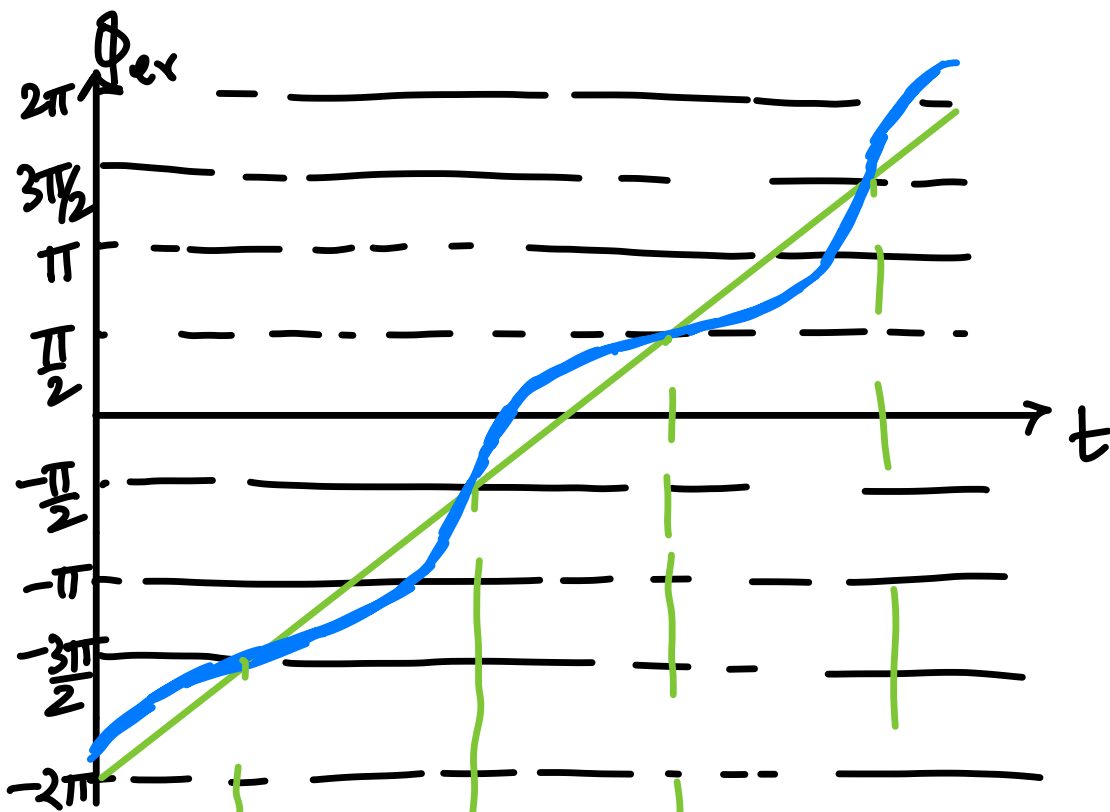
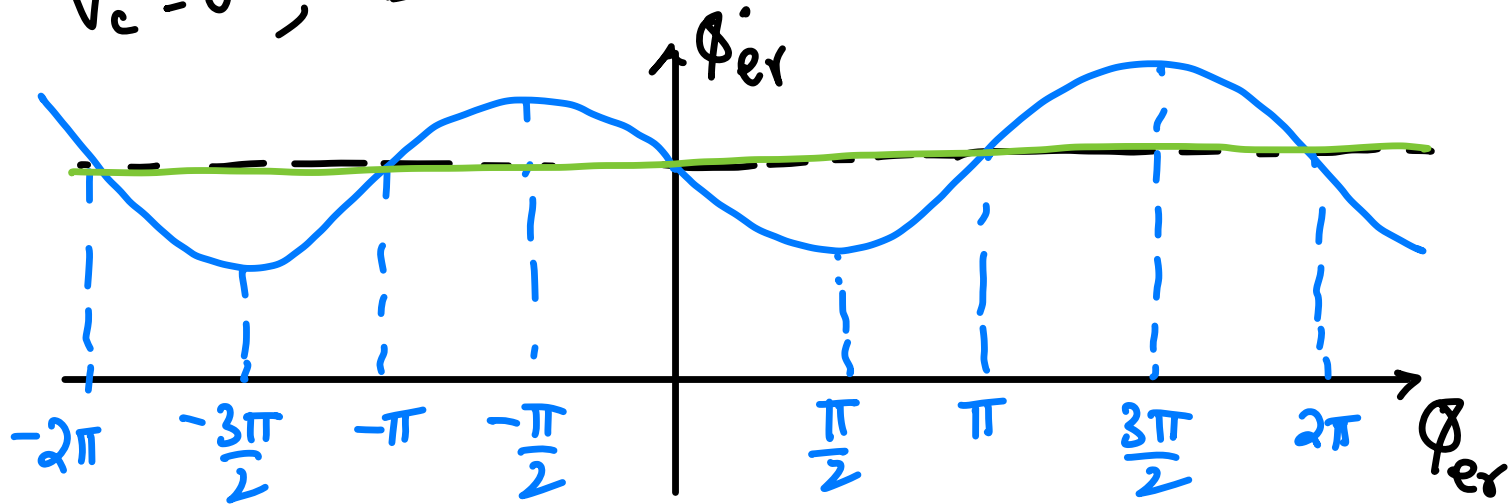
$\Rightarrow$ lock-in range is

$$\Delta\omega_L = K = K_{PD} K_{VCO}$$

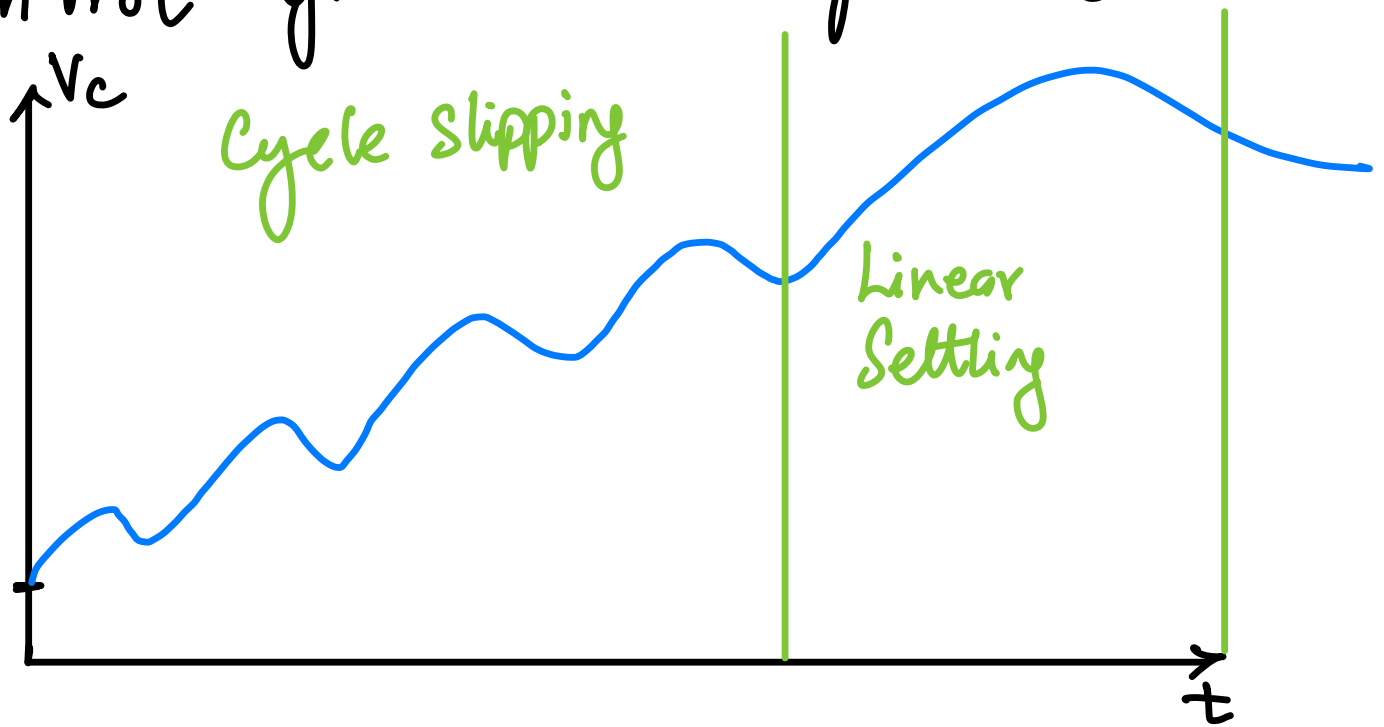
Pull-in Dynamics

Say at $t=0$, $\omega_{in} = \omega$; $\omega_{out} = \omega_{fr}$;

$$V_c = 0; \Delta\omega(\omega) > K$$



Control Systems $\rightarrow$ Integrator!! (PI).



Pull in range $\Leftrightarrow$ VCO Tuning range.
 $\rightarrow$ Hold in range $\nwarrow$