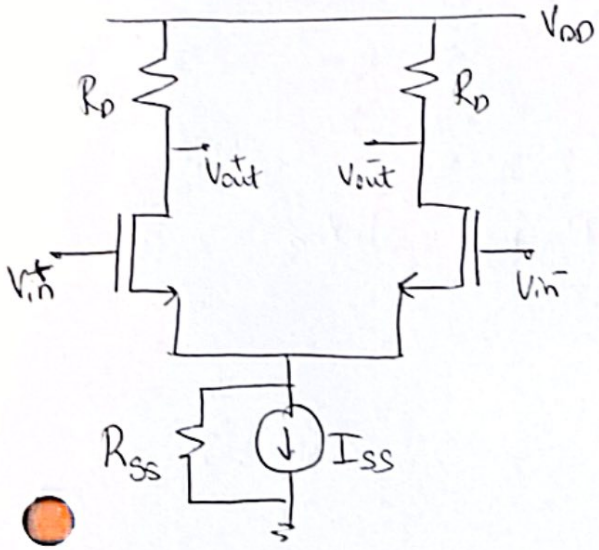
Lec 26 Roadmap to Op-Amps

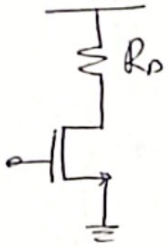
Differential Inputs & Single Ended Output



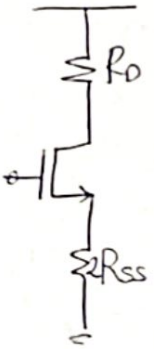
Diff. Mode

Hallf Circuits

Common Mode



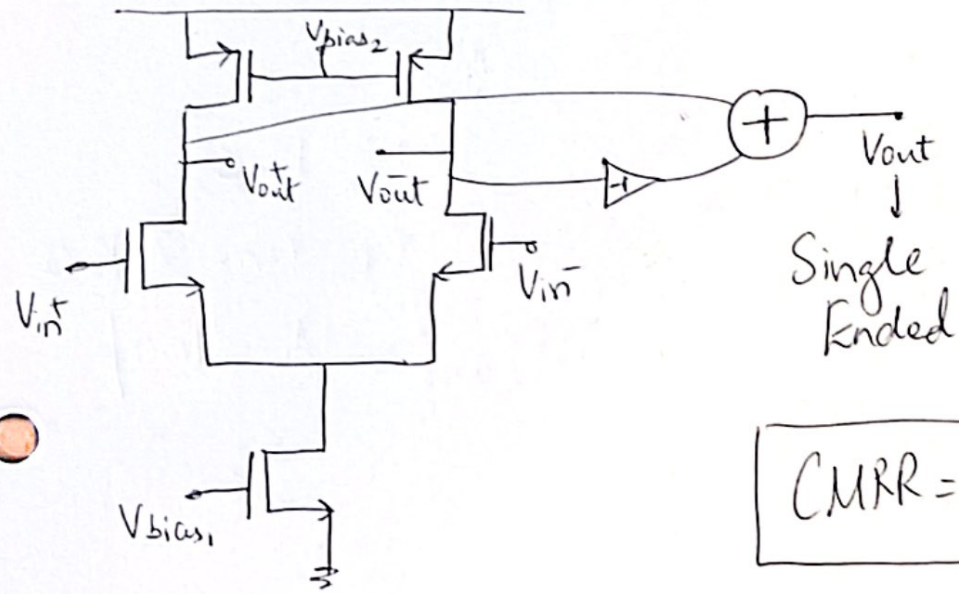
$$A_{v_D} = -g_m(r_o \| R_D)$$



$$A_{v_C} = \frac{-g_m(R_D \| r_o)}{1+2g_m R_{SS}}$$

$$\boxed{CMRR = 1 + 2g_m R_{SS}}$$

More Gain?



Single Ended

$$A_{v_D} = -g_m(r_{on} \| r_{op})$$

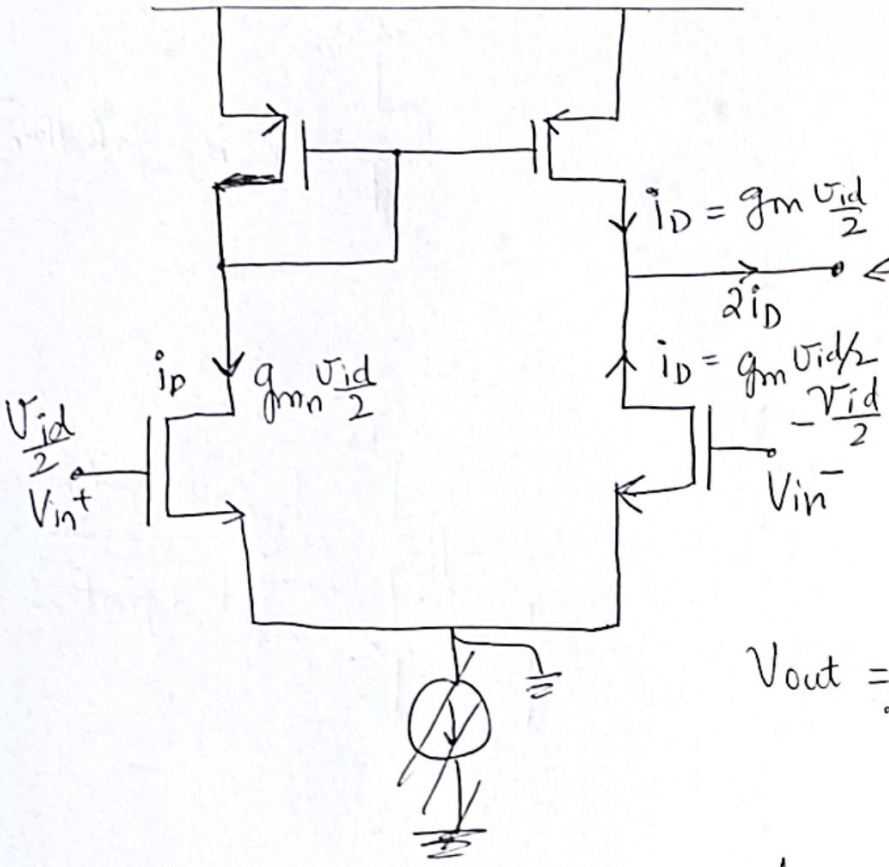
$$A_{v_C} = \frac{-g_m(r_{on} \| r_{op})}{1 + 2g_m r_{on}}$$

$$\boxed{CMRR = 1 + 2g_m r_{on}}$$

> Taking only one output ⇒ $\frac{1}{2}$ gain & very low CMRR.

> How can we implement the Diff → Single Ended network?

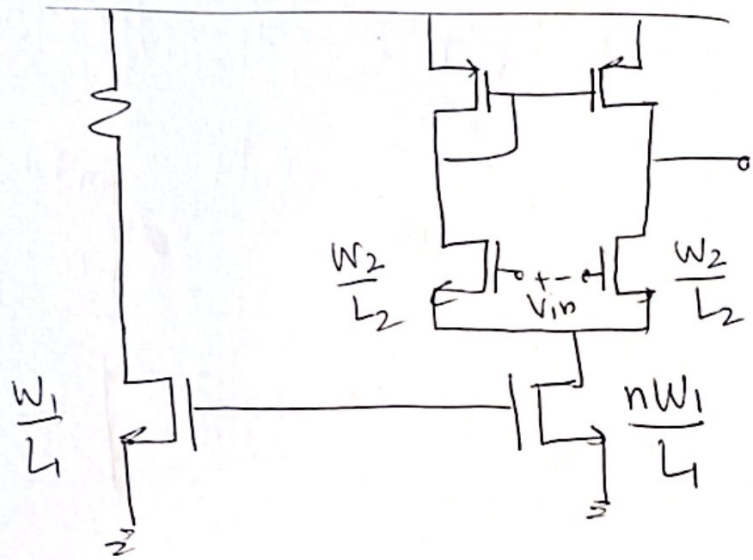
Use Current Mirrors!



$$V_{out} = 2\left(\frac{g_m v_{id}}{2}\right)(r_{op} \| r_{on})$$

$$\Rightarrow A_v = g_m (r_{op} \| r_{on})$$

>



$g_m = 10m\,S$

$r_{op} = r_{on} = 20K\,\Omega$

$\Rightarrow$ Large

$\Rightarrow$ $A_v = 100$

OK

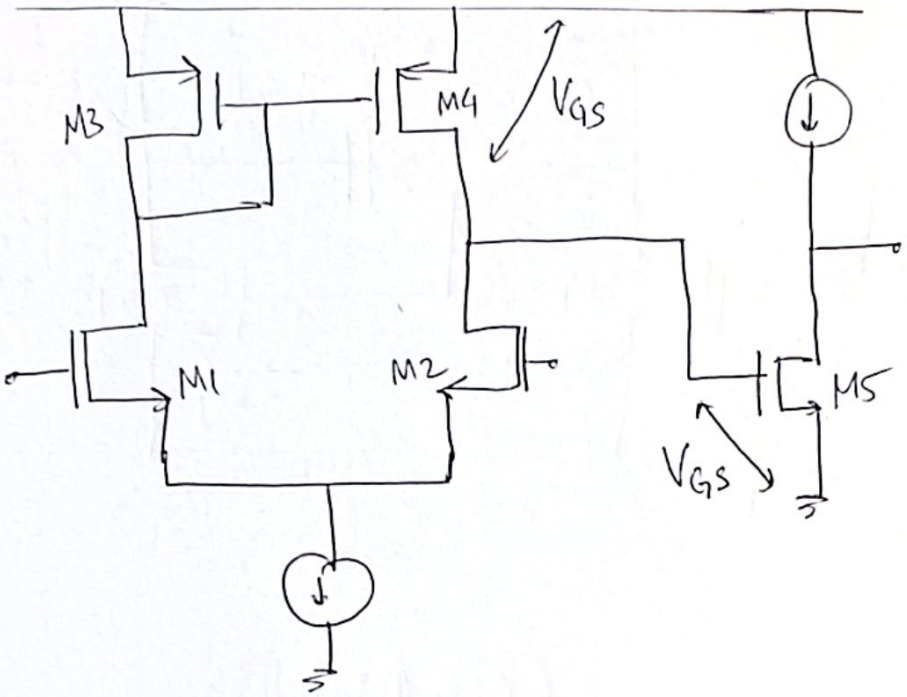
> To drive a low impedance load, say $R_L = 50\Omega$.

> Use Common Drain Buffer.

> For more gain, we need what? Too much headroom.

Cascode diff pair?

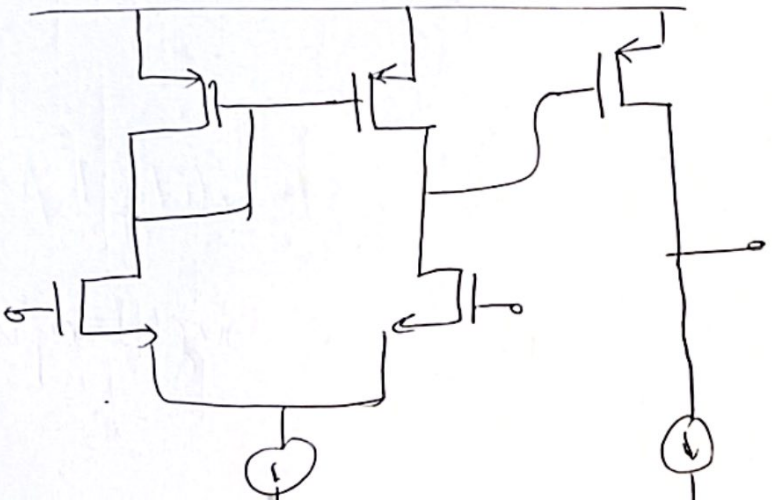
Common Source Stage?



> Biasing is a problem

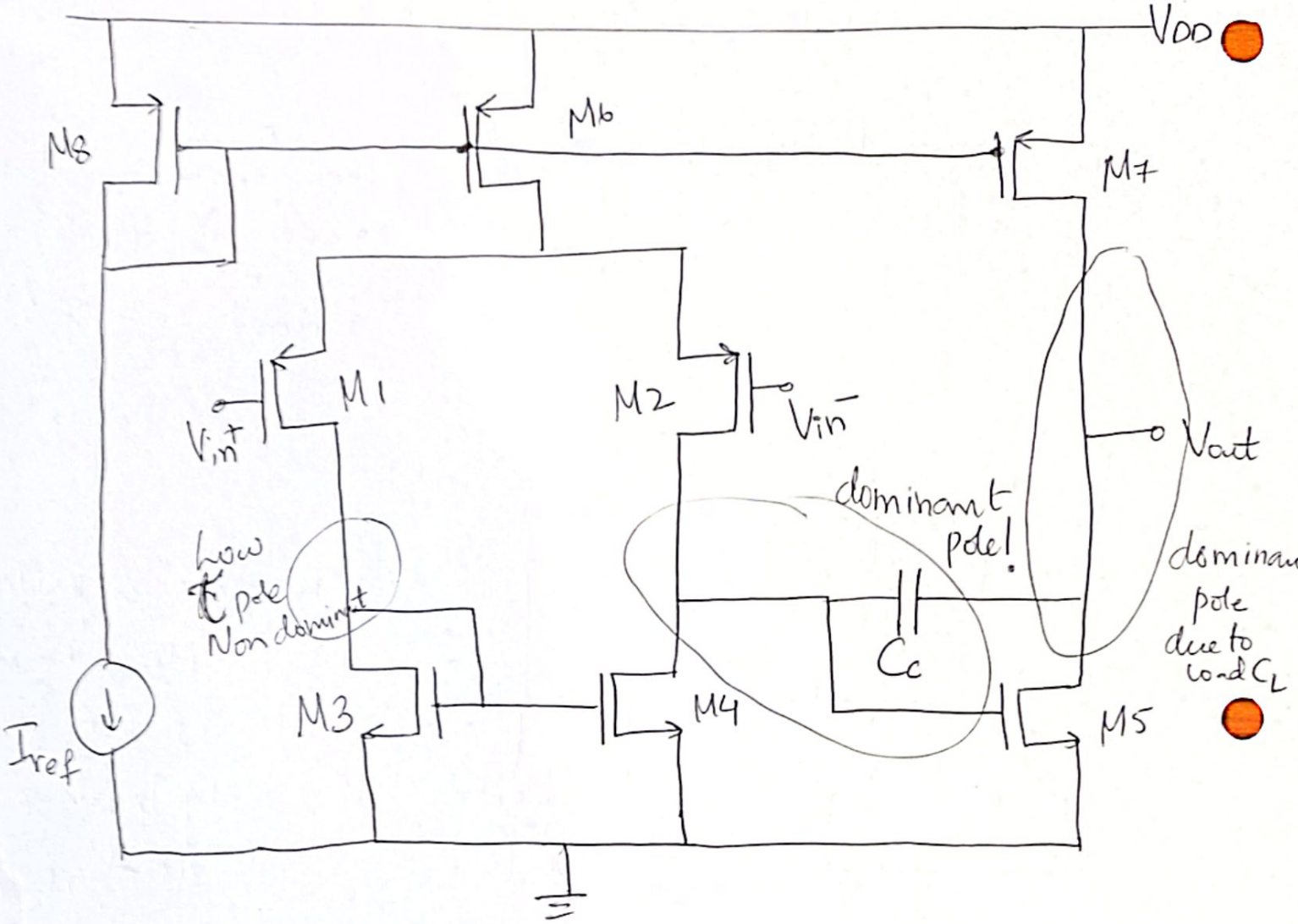
Since M_5 gate is at V_{GS} but M_4 Drain is at $V_{DD} - V_{GS}$

Fix? Use PMOS Common Source!



> In opamps for Stability we want Stage ① gain to be low & Stage ② gain to be high so we infact use PMOS for stage ① & NMOS for Stage ②.

8-Transistor Op-Amp



Gain: $\{gm_{P_1}(r_{on_1} \| r_{op_3})\}\{gm_{n_5}(r_{on_5} \| r_{op_7})\}$

$\approx 10^4$

> 3 poles & 2 zeroes → Bad for stability! Add Cc.

> Noise analysis & Stabilization using Compensation Cap → EE140!

Course Overview

- ① Circuits & Systems
  - Circuit Fundamentals
    - KVL, KCL
    - Theorems
  - ↓
  - LTI Systems
    - Impulse Response
    - Frequency Response, Poles/Zeros
    - Laplace Transforms.
  - ↓
  - Feedback & Non ideal op-amps.

- ② Device Physics
  - Semiconductor Physics
    - Drift, Diffusion
  - PN Junc.
  - BJT
  - MOS
    - Large Signal Models.
    - Small Signal Models

- ③ Amplifier Design
  - Single Stage
  - Biasing
  - Frequency Analysis
  - Multistage
  - Diff Pair
  - Op-Amps

Final Exam

Q1 : 15 Short Answer

Q2 : Part ①

Q3 : Part ②

Q4 : Part ③

Q5 : Part ④

Q6 : Design Problem