EE105 – Microelectronic Devices and Circuits
Spring 2026, Homework #9

Assigned: **April 7, 2026**
Due: **April 14, 2026 at 11:59 PM on Gradescope**

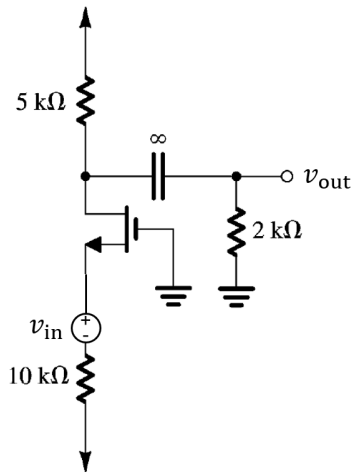
1 Notes

Upload your notes from Lectures 18 and 19.

2 Problem Set

2.1 Problem 1: Single-Stage Amplifier with Input Source Transformation

Consider the single-stage amplifier topology below with $g_m = 15\,\text{mA/V}$. In this problem, for small signal models and all calculations, you may assume $\lambda = 0$.



(a) What amplifier topology is this? What is its common "nickname" and why?

(b) Draw the small-signal AC model of the circuit.

(c) What is the voltage gain $\frac{v_{out}}{v_{in}}$ (numerical answer)?

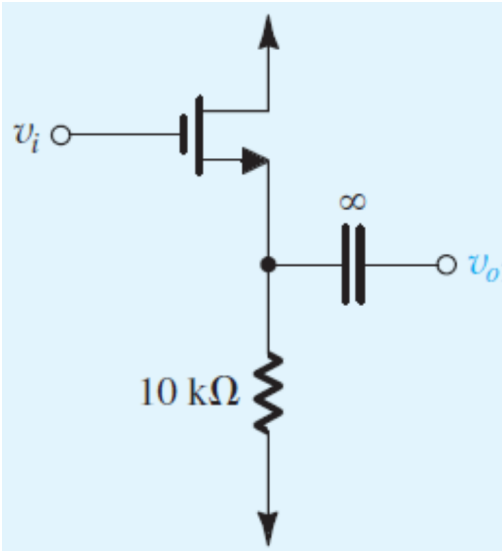
(d) Using source transformation to convert v_{in} into a current source i_{in}, redraw the new small-signal AC model.

(e) Calculate the gain $\frac{v_{out}}{i_{in}}$ (numerical answer).

(f) Calculate the input impedance of this circuit (provide a numerical answer) considering the 10 kΩ resistor to be part of the input source (source resistance).

2.2 Problem 2: Another Single-Stage Amplifier!

Consider the single-stage amplifier topology below. The drain is connected to a DC voltage source to maintain operation in the saturation region of the NMOS FET.
The NMOS transistor in the circuit has $g_m = 10\,\text{mA/V}$ and $r_o = 10\ \text{k}\Omega$.



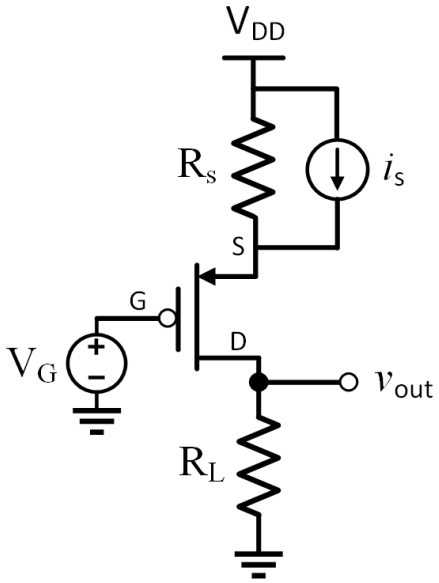
(a) What amplifier topology is this? What is its common "nickname" and why?

(b) Draw the small signal model, calculate the gain $\frac{v_o}{v_i}$, and the amplifier's output impedance Z_{out}.

(c) Now using, the appropriate two-port model from Fig 12.21 of the reader, redraw this circuit in two-port model form.

(d) Using the two-port model, recalculate the gain $\frac{v_o}{v_i}$, and the output impedance Z_{out}. How different is this result than the one calculated in part (b)? Comment on the potential benefits/ disadvantages of using such two-port models?

2.3 Problem 3: PMOS Single-Stage Amplifier



(a) What amplifier topology is this?

(b) If r_o is very large (can be modeled as an open circuit) and you can ignore body effect, draw the small-signal model corresponding to the circuit.

(c) What is the small-signal gain $\frac{v_{out}}{i_s}$? Leave the answer in terms of R_s, R_L, and g_m.

(d) Given $V_G = 0\,\text{V}$, $R_S = 3\,\text{k}\Omega$, $V_{DD} = 12\,\text{V}$, $V_{Tp} = -3\,\text{V}$, and $k_p = \frac{\mu C_{ox} W}{L} = 0.75\,\text{mA/V}^2$, solve for V_S and I_{SD}.

(e) For the transistor to remain in saturation, what is the maximum allowable large signal V_D? What is the corresponding R_L?

2.4 Problem 4: Leveraging Back-Gate/Body Transconductance

Assume that the following circuit has:

$$V_{Tn} = 1\,\text{V (without body bias)}$$

$$k_n = \frac{\mu C_{oxe} W}{L} = 10^{-3}\,\text{A/V}^2$$

$$\lambda = 0$$

$$\gamma = 0.5\,\text{V}^{1/2}$$

$$\phi_p = -400\,\text{mV}$$

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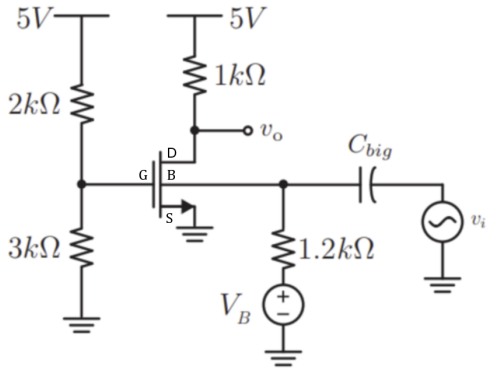
C_{big} means the AC-coupling capacitor acts as a high frequency filter only allowing AC signals to "pass through". It is very large, therefore we can treat it as a short circuit for small-signal calculations (while still keeping it an open circuit for DC biasing calculations).



(a) What amplifier configuration would you qualify this circuit to be and why?

(b) If $V_B = -1.5\,\text{V}$, calculate V'_{Tn}, g_m and g_{mb} (numerical answer).

Hint: Leverage the following relationship to calculate g_{mb}: $\frac{C_{dep}}{C_{oxe}} = \frac{\gamma}{2\sqrt{-V_{BS} - 2\phi_p}}$.

(c) Draw the AC small-signal model for this circuit, considering the body effect and that $\lambda = 0$.

(d) Derive and compute the corresponding voltage gain $\frac{v_o}{v_i}$ (numerical answer).

(e) If V_B was decreased to $-2\,\text{V}$, would the magnitude of the gain of this circuit increase or decrease? (No need to recalculate the gain; a short explanation is sufficient).