EE105 – Microelectronic Devices and Circuits
Spring 2026, Homework #4

Assigned: **February 17, 2026**
Due: **February 24, 2026 at 11:59 PM on Gradescope**

1 Notes

Upload your notes from Lectures 8 and 9.

2 Problem Set

2.1 Problem 1: Finite Gain and Bandwidth Op-Amp

Consider the negative feedback network shown below. The Op-Amp has finite gain and bandwidth, and its open-loop transfer function $A(s)$ is modeled as a single-pole system:

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_p}}$$

where A_0 is the open-loop DC gain and ω_p is the open-loop pole frequency/ 3dB frequency.

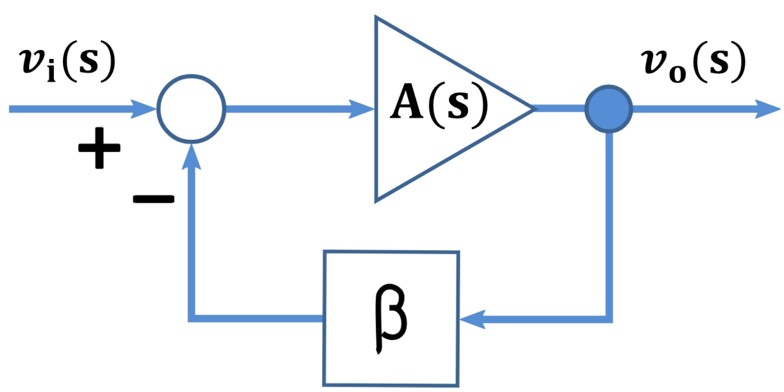

Figure 1: Negative feedback network.

(a) Derive the closed-loop input-to-output transfer function in terms of A_0, ω_p, and β.

(b) Determine the closed-loop DC gain (often denoted A_{CL}) and the closed-loop pole/3 dB frequency ω_{CLp} in terms of A_0, ω_p, and β.

Hint: It may be helpful to arrange the transfer function obtained in part (a) in standard first-order form.

(c) Knowing that A_0 is usually a large and unstable value, compare the open-loop gain with the closed-loop gain. Compare the open-loop bandwidth with the closed-loop bandwidth. Comment on the benefits of negative feedback in amplifier circuits.

In lecture, we have learned that if A_0 and ω_p are infinitely large, then the input to output gain/transfer function can be simplified to $\frac{1}{\beta}$.

(d) If I consider the gain to be $\frac{1}{\beta}$ instead of the actual value calculated in (d), what error would I observe for a low frequency input signal (can ignore effect of pole)? Answer in terms of A_0, and β.

Hint: Use the following equation for percent error calculation

$$error = \frac{x_{\text{estimated}} - x_{\text{real}}}{x_{\text{real}}} \times 100\%$$

(e) If $\beta = \frac{1}{100}$, what is the minimum open-loop DC gain A_0 spec for the Op-Amp to ensure a maximum of 1% error at low frequencies?

(f) You are now told that open-loop loop pole/3 dB frequency ω_p has a value of 100 $krad/s$. With the given value of $\beta = \frac{1}{100}$, the minimum open-loop DC gain A_0 solved in part (e) and the equation for ω_{CLp} solved in part (b); calculate the numerical value for the closed-loop loop pole/3 dB frequency ω_{CLp}.

(g) A step input $v_i(t) = 2\ u(t)$ is applied to the closed-loop system.
Draw the output $v_{out}(t)$ as a function of time after the step is applied. Label numerical values for x and y-axes at $t = \tau,\ 3\tau,\ 5\tau$.

Hint: Recall the output voltage will be of the form $v_{out}(t) = V_{final}(1 -\ e^{\frac{-t}{\tau}})$ where V_{final} is determined by the amplitude of the step input and the DC gain of the closed-loop system. The time constant τ is defined as the inverse of the closed-loop loop pole/3 dB frequency ω_{CLp}.

2.2 Problem 2: Active Filter

Consider the op-amp in the figure below to be ideal (infinite input impedance, zero output impedance, infinite gain, infinite bandwidth, no offset or slew rate limitation).

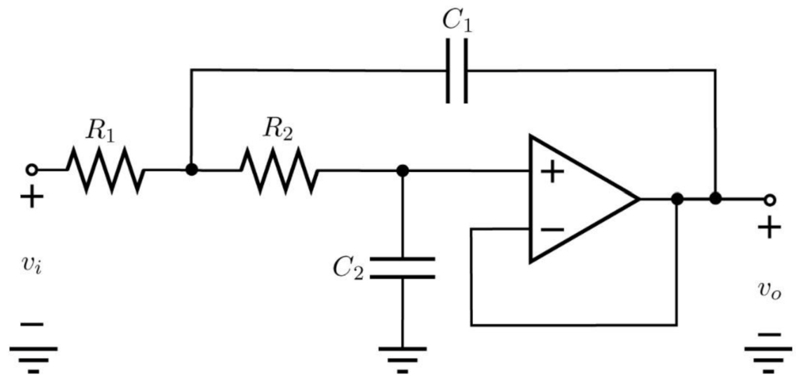

Figure 2: Op-amp filter circuit.

(a) Find the transfer function

$$\frac{v_o(s)}{v_i(s)}$$

in terms of the circuit parameters (R_1, R_2, C_1, C_2).

Hint: In an ideal op-amp, no current flows into or out of either of the + and − input terminals. Symbolically, $i_+ = i_- = 0$.

Hint: In negative feedback, the voltage at the input terminals $(+$ *and* $-)$ *are equal. Symbolically,* $v_+ = v_-$ *and* $v_{in} = 0$.

(b) Now, consider $C_1 = C_2 = C$ and rewrite the transfer function. How many poles and/or zeros does the transfer function have? What are the frequencies corresponding to the poles and/or zeros?

(c) For $R_1 \gg R_2$, draw the magnitude and phase Bode plots for this transfer function labeling relevant magnitudes, phases, frequencies, and asymptotic values. What kind of filter is this?

2.3 Problem 3: Input Offsets and Slew-Rates

With "real" op-amps in negative feedback, a DC differential voltage can exist between the inverting and non-inverting terminals due to input transistor mismatch. This "offset voltage" can be modeled by adding a voltage source and/or a current source at the non-inverting terminal and/or the inverting terminal of an otherwise ideal op-amp. Here, they are highlighted in yellow in Figure 3 and modeled with a DC voltage source V_{os} and a DC current source I_{os} at the non-inverting terminal. The input voltage source V_s has a parasitic series resistance R_s.

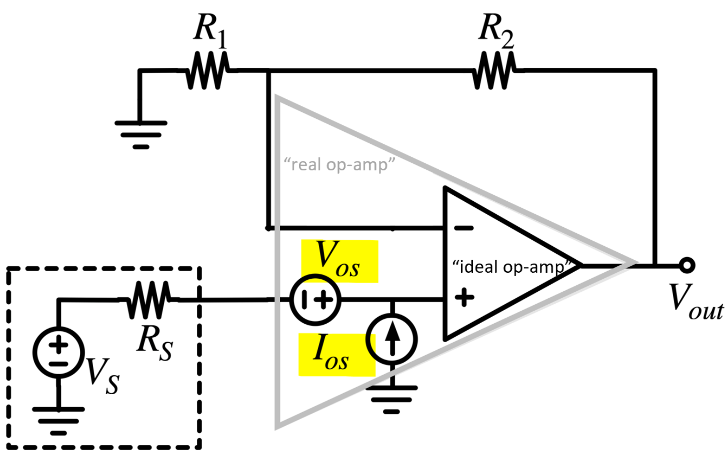

Figure 3: Op-amp circuit with input voltage offset.

(a) Find v_{out} as a function of the circuit paramaters R_1, R_2, V_{os}, I_{os}, V_s and R_s.

Hint: There can be many ways to go about this: using superposition, KCL, key op-amp transfer functions, or a mixture of the aforementioned methods. In either way, leverage negative feedback ideal op-amp rules: $i_+ = i_- = 0$ *and* $v_+ = v_-$

(b) You are told that $R_2 = 9\text{k}\Omega$, $R_1 = 1\text{k}\Omega$, $R_s = 1\Omega$, $V_{os} = 5\text{mV}$, $I_{os} = 5\text{mA}$. A step input is applied such that $v_s = u(t)$. Using the equation found in part (a), calculate the v_{out} before the step is applied and its final steady-state value after the step has been applied.

(c) You are told that the op-amp has a maximum slew rate of $1\frac{V}{\mu s}$. Draw the output $v_{out}(t)$ for $t \geq 0$ s, labeling the time at which it reaches its final value.

2.4 Problem 4: Semiconductor Basics

(a) Briefly describe the difference between metal, semiconductor, and insulator materials using the energy band model (drawings are expected).

(b) What are the free electrons and holes in a semiconductor?

(c) What is the probability of an electron being at an energy $3kT$ higher than E_f?

(d) Consider a Silicon sample placed in a room with a temperature of 0 K. An electric field is applied to it. What is the resulting current? Why?